

Please amend Claim 1 as follows.

1           1.    **(Currently Amended)** During the testing of the  
2 operation of processing unit, a system for identifying the  
3 occurrence of an interrupt service routine code flush  
4 condition in ~~the~~ a pipeline flattener, the system  
5 comprising:

6           timing trace apparatus responsive to signals from the  
7 processor unit, the timing trace apparatus generating a  
8 timing trace stream;

9           program counter trace apparatus responsive to signals  
10 from the processing unit, the program counter trace  
11 apparatus generating a program counter trace stream; and

12           synchronization apparatus applying periodic signals to  
13 the timing trace apparatus and to the program counter trace  
14 apparatus, the periodic signals resulting in periodic sync  
15 markers in the timing trace stream and in the program  
16 counter trace stream.

17           wherein the program counter trace apparatus is  
18 responsive to an interrupt service routine code flush  
19 signal, the program counter trace apparatus generating a  
20 sync marker signal group identifying the occurrence of the  
21 interrupt service routine code flush signal and relating  
22 the interrupt service routine code flush signal to the  
23 timing trace stream and to ~~the~~ program code execution.

24           2.    **(As Filed)**       The system as recited in claim 1  
25 wherein the marker signal group includes a program counter  
26 address, a timing index and a periodic sync ID.

**Please amend Claim 3 as follows.**

1        3.    (**Currently Amended**) The system as recited in  
2 claim 1 further comprising:

3        a data trace apparatus responsive to signals from the  
4 processing unit, the data trace apparatus generating a data  
5 trace stream, wherein the periodic signals are applied to  
6 the data trace apparatus resulting in periodic sync markers  
7 in the data trace stream; and

8        a host processing unit, the host processing unit  
9 responsive to the timing trace stream, the program counter  
10 trace stream and the data trace stream, the host processing  
11 unit reconstructing the ~~processing activity~~ the program  
12 code execution of the processing unit from the trace  
13 streams.

**Please amend Claim 4 as follows.**

14       4.    (**Currently Amended**) The method for communicating  
15 an occurrence of an interrupt service routine code flush  
16 signal from a target processor unit to a host processing  
17 unit, the method comprising:

18       generating a timing trace stream, a program counter  
19 trace stream, and a data trace stream, and

20       in the program counter trace stream, including an  
21 interrupt service routine code flush sync marker signal  
22 group indicating an occurrence of an interrupt service  
23 routine code flush signal and relating the occurrence to  
24 the data trace stream and to the timing trace stream.  
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1           5.    **(As Filed)**       The method as recited in claim 4  
2 further including:  
3           including periodic sync markers in the timing trace  
4 stream and in the program counter trace stream; and  
5           including in the program code sync marker reference to  
6 a periodic sync marker.

**Please amend Claim 6 as follows.**

7           6.    **(Currently Amended)** In a processing unit test  
8 environment wherein a target processor transmits a  
9 plurality of trace streams to a host processing unit, an  
10 interrupt service routine code flush sync marker signal  
11 group included in a trace signal stream, the target  
12 processor including a target processor clock, the marker  
13 signal group comprising:  
14           an indicia of the occurrence of an interrupt service  
15 routine code flush signal;  
16           an indicia of the relationship of the occurrence of  
17 the interrupt service routine code flush signal to the  
18 target processor clock; and  
19           an indicia of the relationship of the occurrence of  
20 the interrupt service routine code flush signal to ~~the~~ a  
21 target processor program execution.

**Please amend Claim 7 as follows.**

22           7.    **(Currently Amended)** In a target processing unit  
23 generating trace test signals for transfer to a host

1 processing unit, a program counter trace generation  
2 apparatus comprising:

3 sync marker assembly apparatus, the sync marker  
4 assembly apparatus including:

5 a storage unit;

6 a decoder unit responsive to an interrupt service  
7 routine code flush signal for storing an indicia of ~~the~~ an  
8 interrupt service routine code flush signal in the storage  
9 unit, the decoder unit generating a ~~controls~~ control  
10 signal;

11 a gate unit having a timing index, a periodic  
12 sync signal, and a program counter address, the gate unit  
13 storing the timing index, the periodic sync signal and the  
14 program counter address in the storage unit; and

15 a FIFO unit, the storage unit transferring the  
16 stored signals to the FIFO unit in the form of a program  
17 code flush sync marker.

18 8. (As Filed) The program counter trace  
19 apparatus as recited in claim 7 responsive to a selected  
20 control signal for transferring the interrupt service  
21 routine code flush marker in the FIFO unit to an output  
22 port of the target processor.

23 9. (As Filed) The program counter trace  
24 apparatus as recited in claim 8 wherein the apparatus can  
25 form a periodic sync marker in response to a periodic sync  
26 signal.

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Please amend Claim 10 as follows.

1        10. (**Currently Amended**) The program counter trace  
2 apparatus as recited in claim 9, wherein the target  
3 proccession unit includes a pipeline flattener, wherein the  
4 interrupt service routine flush signal indicates the change  
5 from a first instruction code sequence to a second  
6 instruction code sequence exiting the pipeline flattener.

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8        11. (**As Filed**) The program counter trace  
9 apparatus as recited in claim 10 wherein the first  
10 instruction code sequence is an interrupt service routine  
11 code and the second instruction sequence is a program code.

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